CLAIMS:

What is claimed is:

1. A device for storing information including an array of memory cells, said device comprising:

bitlines and wordlines for addressing the memory cells, said bitlines being subdivided into sectioned bitlines for sections of wordlines;

a plurality of global bitlines; and

a connector connecting sectioned bitlines to a global bitline, said connector being bidirectional and using the high order part of the wordline addresses for a section of bitlines as a disable reset command such that the reset stays active for unselected portions of the array thereby compensating leakage of a mass of unselected memory cells which could disturb valid read signals.

2. The device according to claim 1, wherein said bitlines are precharged to power rail voltage.

3. The device according to claim 1, wherein said global bitlines are precharged to ground.

4. The device according to claim 1, wherein said disable reset command is delayed when writing to a memory cell thereby avoiding pre-setting the global bitline by reading the memory cell.

5. The device according to claim 1, wherein said disable reset command is split and controlled by the signals selecting one of several bitlines driving toward the memory output in order to maintain unselected bitlines in precharged condition.

6. The device according to one claim 1, wherein said bitlines and said global bitlines are both dual railed.

7. The device according to claim 1, further comprising a precharged p-type domino circuit driving said global bitlines from bitlines.

8. The device according to claim 1, further comprising a high order word address disabling local reset gating a write command such that the resulting signal connects one pair of bitlines to its pair of global bitlines thereby minimizing the number of devices for write, and a minimal number of bitlines are discharged thereby reducing power consumption.

9. The device according to claim 1, wherein the disabling of the local reset is delayed during writing.

10. The device according to claim 1, wherein the bitlines are subdivided in sections with equal numbers of wordlines.

11. The device according to claim 1, further comprising a gate splitting the disable reset command into individual signals per bitline by gating with the bitline select signals.

12. A method for partial write for storing information in a device including an array of memory cells, said method comprising:

organizing the array with bitlines and wordlines for addressing the memory cells;

subdividing said bitlines into sectioned bitlines for sections of wordlines; and

connecting sectioned bitlines to one of global bitlines, said connector being bidirectional and using the high order part of the wordline addresses for a section of bitlines as a disable reset command such that the reset stays active for unselected portions of the array thereby compensating leakage of a mass of unselected memory cells which could disturb valid read signals.

13. The method according to claim 12, further comprising precharging said bitlines to power rail voltage.

14. The method according to claim 12, further comprising precharging said global bitlines to ground.

15. The method according to claim 12, further comprising delaying said disable reset command when writing to a memory cell thereby avoiding pre-setting the global bitline by reading the memory cell.

16. The method according to claim 12, further comprising splitting said disable reset command and controlling said reset command by the signals selecting one of several bitlines driving toward the memory output in order to maintain unselected bitlines in precharged condition.

17. The method according to one claim 12, wherein said bitlines and said global bitlines are both dual railed.

18. The method according to claim 12, further comprising precharging a p-type domino circuit for driving said global bitlines from bitlines.

19. The method according to claim 12, further comprising gating a write command with a high order word address disabling local reset such that the resulting signal connects one pair of bitlines to its pair of global bitlines thereby minimizing the number of devices for write, and a minimal number of bitlines are discharged thereby reducing power consumption.

20. The method according to claim 12, further comprising delaying the disabling of the local reset during writing.

21. The method according to claim 12, wherein the bitlines are subdivided in sections with equal numbers of wordlines.

22. The method according to claim 12, further comprising splitting the disable reset command into individual signals per bitline by gating with the bitline select signals.